UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,523	11/29/2001	Vishal Sharma	04910000012	5357

23418 7590 06/28/2005

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
NGO, NGUYEN HOANG	
ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,523	VISHAL SHARMA	
	Examiner	Art Unit	
	Nguyen Ngo	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____:

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 2 and 3 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. Claim 2 recites the limitation "the data buffers" in line 3. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 3 recites the limitation "the data buffers" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7 and 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Cisneros (U.S 5,157,654), hereinafter referred to as Cisneros.

Regarding claim 1, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said data queues also having an output coupled to a corresponding input of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (plurality of data demultiplexers, each having a data input port at which a data stream is received, and each demultiplexer having a plurality of data outputs, each of which is coupled to a corresponding single input of said plurality of input data queues associated with each cross bar switch input, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler, coupled to

said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

Regarding claim 2, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said data queues also having an output coupled to a corresponding input of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (plurality of data demultiplexers, each having a data input port at which a data stream is received, and each demultiplexer having a plurality of data outputs, each of which is coupled to a

corresponding single input of said plurality of input data queues associated with each cross bar switch input, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler, coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

a header processing unit formed of input buffer which provides sufficient time to perform table look up operations to translate the current VCI for an incoming cell and formulate an appropriate routing header for that cell in conjunction with the switch control module (col15 lines 35-56) and that the routing header is strictly for internal use in routing the entire cell through the switch (examining cells at the heads of the data buffers and determine from data in said cells, which input port of a cross bar switch should be coupled to a particular output port of the crossbar switch, col11 lines50-59).

Regarding claim 3, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said data queues also having an output coupled to a corresponding input of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (plurality of data demultiplexers, each having a data input port at which a data stream is received, and each demultiplexer having a plurality of data outputs, each of which is coupled to a corresponding single input of said plurality of input data queues associated with each cross bar switch input, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler, coupled to said data demultiplexers and to each of said data input data queues, controlling the routing of data from said plurality of switch input ports to said plurality of switch output ports, col12 lines56-68).

a header processing unit formed of input buffer which provides sufficient time to perform table look up operations to translate the current VCI for an incoming cell and formulate an appropriate routing header for that cell in conjunction with the switch control module (col15 lines 35-56) and that the routing header is strictly for internal use in routing the entire cell through the switch (examining cells at the heads of the data buffers and determine from data in said cells, which input port of a cross bar switch should be coupled to a particular output port of the crossbar switch, col11 lines50-59).

that the header processing unit is connected to the switch control module for receiving control instructions which controls the demultiplexing of the cell traffic on the line across separate lines (col15 line 11-14), and the header processing unit translates the current VCI with the new VCI and prepends an appropriate routing header onto the cell for routing (configure said data demultiplexers so as to route data cells of a particular incoming data flow to an appropriate input data buffer, col15 lines 29-32).

Regarding claim 4, Cisneros discloses an apparatus comprising:

planes of self-routing cross-points switching planes (cross bar switches, 550 of figure 5) with each plane having separate input and separate output connections (each cross bar switch having a plurality of switch input ports and a plurality of switch output ports, col17 lines 57-60).

input modules, wherein each input modules contains a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein

the input modules feeds the input of each of the different switching planes (a plurality of input data queues, each input data queue having an input port capable of receiving data packets, each of said data queues also having an output coupled to a corresponding input of a corresponding cross bar switch, 260 of figure 5 and col19 lines3-6).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules (plurality of data demultiplexers, each having a data input port at which a data stream is received, and each demultiplexer having a plurality of data outputs, each of which is coupled to a corresponding single input of said plurality of input data queues associated with each cross bar switch input, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (a scheduler means, coupled to said data demultiplexers and to each of said data input data queues and to the cross bar switches, col12 lines56-68).

of a demultiplexer that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams. Each of these streams feeds into four different corresponding input ports. That the STS-12 ATM cells, which are provided to the input ports of the associated input module, are sequentially entered in a regular order into a single internal queue within that module, are also read from a single

corresponding logical queue in a common output module in the same order, which will advantageously preserve the ordering of the bits on the STS-12 trunk entirely through the switch (dividing the delivery of data packet of data flows of an input data stream that is input to said data switch, and by computing a data packet schedule for each cross bar switch such that the temporal order of data packets into said data switch is maintained through each of the cross bar switches, col50 lines 50-66).

Regarding claim 5, Cisneros discloses a switch fabric comprising:

self-routing cross-point switching planes composed of identical cross-point switching planes (col17 lines 35-40) with each plane having 256 separate input and 256 separate output connections (a plurality of K cross bar switches, each switch having N switch input ports I, and N switch output ports O, 550 of figure 5 and col17 lines 57-59).

input modules, containing a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein for any input module, each successive incoming line in the group is connected to a corresponding successive input port of that module and in addition, each of the input modules is connected to the same corresponding numerical input port on all of cross-point switching plane (N, parallel input data buffers B, each input data buffer B having an input port I, each input buffer of said N buffers further having an output O coupled to a single one of said N crossbar switch input ports such that data packets in each of said N, parallel input buffers can be selectively routed into said crossbar switch, 250 of figure 5 and col18 59-68).

output modules, containing a single queue, which feeds from the cross-point switching planes. Each of the numerical outputs on any one of the switching planes feeds a common numerical input on every output module (col19 lines 22-26). Each of the output modules routes incoming switched ATM cells to one of the separate output ports available on that module which is connected to a corresponding output line (an output buffer, each output buffer having an input coupled to a single one of said N outputs of the corresponding crossbar switch and each output buffer having an output port from which data is transmitted to an output destination link, 270 of figure and col19 lines 45-49).

demultiplexers which accepts incoming cells from user lines and demultiplexes the cells occurring at the STS-48 rate and appearing on single incoming lines, on a 1-to-16 basis, into separate bit-serial lines feeding the input modules containing input ports I and a single queue (N data demultiplexers comprising of a data input port at which a data stream S is received, and N data output ports, each data output port being coupled to the input I of a corresponding single one of said input data buffers, each of said data demultiplexers selectively routing certain data packets in said stream S to at least one input data buffer, 230 of figure 2 and col13 lines48-55).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (a scheduler coupled to said N data demultiplexers, cross bar switches, and said N data input data buffers, said

scheduler controlling the selective delivery of data packets into certain input data buffers and from said input data buffers into a corresponding crossbar switch, 290 of figure 2 and col12 lines56-68).

Regarding claim 6, Cisneros discloses a switch fabric comprising:

self-routing cross-point switching planes composed of identical cross-point switching planes (col17 lines 35-40) with each plane having 256 separate input and 256 separate output connections (K cross bar switches, each of said K switches having N switch inputs I and N switch outputs O, 550 of figure 5 and col17 lines 57-59).

input modules, containing a single queue, that successively reads the current incoming ATM cells appearing at each of its inputs and deposits the cell into the next available location in the queue (col20 lines 9-16), wherein for any input module, each successive incoming line in the group is connected to a corresponding successive input port of that module and in addition, each of the input modules is connected to the same corresponding numerical input port on all of cross-point switching plane (250 of figure 5 and col18 59-68) and reads a cell from the head of its internal queue (N input data FIFO buffers, each input data FIFO buffer having an input to which stream of data can be sent, each input data FIFO further having an output Bo coupled to a single input Ij of said N input ports, each of said input data FIFO buffers storing data packets to be routed through the cross bar switching system from input Ij to an output Ok, 250 of figure 5 and col20 lines 26-30).

a demultiplexer, containing input and output ports, that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams. Each of these streams feeds into four different corresponding input ports. That the STS-12 ATM cells, which are provided to the input ports of the associated input module, are sequentially entered in a regular order into a single internal queue within that module, are also read from a single corresponding logical queue in a common output module in the same order, which will advantageously preserve the ordering of the bits on the STS-12 trunk entirely through the switch (N data demultiplexers, each data demultiplexer having a data input port at which a data stream S comprised of a plurality of data flows is received, and further having N data output ports, each data output port of each demultiplexer being coupled to corresponding ones of the inputs of the input data FIFO buffers at each input of said K parallel cross bar switches, each of said data demultiplexer selectively routing data packets of predetermined flows to at least one input I of said input data FIFO buffer, 230 of figure 2 and col50 lines 50-66).

a control switch module coupled to the switch fabric containing input modules and coupled to the demultiplexers (figure 2) which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (a scheduler coupled to said N data demultiplexers, said cross bar switches and said N data input data FIFO buffers, said scheduler being capable of directing data packets of at least one data flow, 290 of figure 2 and col12 lines56-68).

Regarding claim 7, Cisneros discloses each input module in the inventive switch has a single internal queue illustratively implemented using shared memory (input data FIFO buffers are comprised of random access memory, col7 lines42-45).

Regarding claim 12, Cisneros discloses a switching system comprising:

cross-point switching planes on a parallel, through time staggered basis (a plurality of parallel-coupled cross-bar switching systems, col8 lines 12-14).

a control switch module coupled to the switch fabric which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler, operatively coupled to and controlling the flow of data into each of said cross-bar switching systems, 290 of figure 2 and col12 lines56-68).

Regarding claim 13, Cisneros discloses a switching system comprising:

cross-point switching planes on a parallel, through time staggered basis (col8 lines 12-14) with each plane having 256 separate input and 256 separate output connections (a plurality of parallel-coupled cross-bar switching systems, each having a plurality of cross bar inputs and cross bar outputs, 550 of figure 5 and col17 lines 57-59).

a control switch module coupled to the switch fabric which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing

and tearing down appropriate virtual connections through the switch (global scheduler, operatively coupled to and controlling the flow of data into each of said cross-bar switching systems, 290 of figure 2 and col12 lines56-68) and that those cells that win arbitration are simultaneously applied by their respective input modules through the cross-point switching planes and routed there through to the addressed output modules for each cell through the input and output ports of the plane (computing at least one match of cross bar switching inputs to cross bar switching outputs, figure 5 and col7 lines 61-64).

Regarding claim 14, Cisneros discloses a switching system comprising:

cross-point switching planes on a parallel, through time staggered basis (col8 lines 12-14) with each plane having 256 separate input and 256 separate output connections (a plurality of parallel-coupled cross-bar switching systems, each having a plurality of cross bar inputs and cross bar outputs, 550 of figure 5 and col17 lines 57-59).

a control switch module coupled to the switch fabric which controls each of the blocks that constitute the switch, for example, processes incoming calls by establishing and tearing down appropriate virtual connections through the switch (global scheduler, operatively coupled to and controlling the flow of data into each of said cross-bar switching systems, 290 of figure 2 and col12 lines56-68) and that those cells that win arbitration are simultaneously applied by their respective input modules through the cross-point switching planes and routed there through to the addressed output modules

for each cell through the input and output ports of the plane (computing at least one match of cross bar switching inputs to cross bar switching outputs, figure 5 and col7 lines 61-64) and that during each staggered time interval, every input module simultaneously provides output port address and cell priority information for the ATM cell presently situated at the head of its internal queue and routes to a specific cross-point plane (during a data cell time slot interval, col8 lines 18-38).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being anticipated by Cisneros (US 5,157,654), in view of Sharma (SHARMA, Vishal; "Flow Management in the Everest OC-48 POS Line Card: A Problem Formulation and a Strawman Solution",

Memorandum to Steven Dunstan, December 8, 1999), hereinafter referred to as Cisneros and Sharma.

Regarding claim 8, Cisneros discloses a method comprising:

of a demultiplexer that would precede input ports and convert an incoming STS-12 serial bit stream into four different STS-3c streams. Each of these streams feeds into four different corresponding input ports. That the STS-12 ATM cells, which are provided to the input ports of the associated input module, are sequentially entered in a regular order into a single internal queue within that module, are also read from a single corresponding logical queue in a common output module in the same order, which will advantageously preserve the ordering of the bits on the STS-12 trunk entirely through the switch (col50 lines 50-66). All the input modules that have won arbitration, on a serial basis, the ATM cells situated at the head of their internal queues onward through a specific cross-point plane which is part of many cross point planes in parallel (col8 lines 34-40) with each plane having separate input and separate output connections (a method of routing data packets of a data stream to a destination through at least one parallel crossbar switch of a plurality of parallel crossbar switches, each crossbar switch having a plurality of N inputs from which data is routed through the switch to one of a plurality of N outputs, each input of each switch capable of selectively receiving data packets that are stored in N parallel data buffer into which data packets for each of said data streams are selectively written, figure 5 and col17 lines 57-60).

that the preprended routing header of an ATM cell is used solely within the switch, contains fields which specify output module address and a specific output port address on that output module to which the cell is destined (reading a header of a data packet in a data flow and determining from said header, a destination to which said data packet from said data flow is to be sent through one of said parallel crossbar switches, col7 lines37-42).

that input modules containing a single queue successively reads the current incoming ATM cell into the next available location in queue (determining the amount of data stored in the data buffers for each of said cross bar switches, col20 lines 9-16) and that the particular ATM cells that are situated at the head of its internal queue positions of the input modules are routed through the cross-point planes to all the corresponding output modules (col20 lines 44-49).

Cisneros however fails to disclose the specific limitation of routing at least some of the data packets of the flow to a data buffer having the smallest amount of data waiting to be routed through its associated cross bar switch. Cisneros does disclose that internal queues are read in a round robin fashion of the input module (col20 lines 15-19) and gives motivation for a algorithm of assigning the ATM cells to queues in order to avoid congestion and delay due to queue build up.

Sharma however discloses an assignment technique that assigns the flow of data to the pipe with the smaller queue length or, if needed, via a round-robin scheme

as mentioned with Cisneros (routing at least some of the data packets to a data buffer having the smallest amount of data, page 10 line 4).

It would have thus been obvious to a person skilled in the art to incorporate the data flow assignment technique disclosed by Sharma with the method of routing ATM cells through a switch comprising cross-point switching planes in parallel disclosed by Cisneros to effectively assign cells to specific queues to avoid congestion and error of data.

Regarding claim 9, Cisneros discloses that the preprended routing header of an ATM cell is used solely within the switch, contains fields which specify output module address and a specific output port address on that output module to which the cell is destined (reading from said header the identity of a data port of said switch to which at least some data packets are to be sent, col7 lines37-42).

Regarding claim 10, Cisneros discloses that the addresses of the currently available idle memory location for a cell is also written into address chain pointers buffer (reading an address pointer value to determine the amount of data stored in parallel data buffers, col32 lines5-15).

Regarding claim 11, Cisneros discloses that by virtue of storing the memory address for the current incoming cell with chain pointers buffer, a corresponding logical queue is

extended within cell buffer to encompass this latest cell. Output counter appropriately increments the address supplied to sequence through all separate input lines (counting memory location in which data is stored, col32 lines 23-30).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Parruck et al. (U.S 2002/0031127), Asynchronous Transfer Mode Switching Architecture Having Connection Buffers.

b) Saidi et al. (U.S 2002/0145974), Method And Apparatus For High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability.

c) Vasudevan et al. (U.S 6085094), Method For Optimizing Spectral Re-Use.

d) Benmohamed et al. (U.S 6147969), Flow Control Method Far ABR Service In An Asynchronous Transfer Mode Network.

e) Aramaki (U.S 5,253,251), Switching System With Time-Stamped Packet Distribution Input Stage and Packet Sequencing Output Stage.

f) Cordell (U.S 5367520), Method and System For Routing Cells In An ATM Switch.

g) Turner (U.S 6788689), Route Scheduling Of Packet Streams To Achieve Bounded Delay In A Packet Switching System.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen Ngo whose telephone number is (571) 272-8398. The examiner can normally be reached on Monday-Friday 7am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W.N
***

Nguyen Ngo
United States Patent & Trademark Office
Patent Examiner AU 2663
(571) 272-8398

RICKY NGO
PRIMARY EXAMINER
9/27/05